IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1, 5, 9, 11, 13, and 14 and ADD new claim 16 in accordance with the following:

1. (CURRENTLY AMENDED) A semiconductor device substrate comprised of a core substrate having, on both main surfaces of which, respective interconnect patterns extending through resin layers, wherein:

the core substrate being of a material having a heat expansion coefficient of 4.0 to 10.6 ppm/°C, the heat expansion coefficient closer to that of a semiconductor chip than the respective heat expansion coefficients of the resin layers and the interconnect patterns, ~~and~~

a resin layer, forming an outermost layer of the semiconductor device substrate on each of the main surfaces thereof, of a material having at least one of a higher strength and a higher elongation than a resin material used for inner resin layers of the semiconductor device substrate and preventing cracking and deformation, of the semiconductor device substrate due to thermal stress occurring between two or more of the core substrate, the inner resin layers, and the interconnect patterns in the semiconductor device substrate, and

an outermost interconnect pattern of the semiconductor device substrate is coated by a resin layer forming an outermost layer of the semiconductor device substrate, and the outermost interconnect pattern having a land exposed through the outermost layer formed of the resin layer.

2. (PREVIOUSLY PRESENTED) The semiconductor device substrate as set forth in claim 1, wherein a further resin layer, under the resin layer forming the outermost layer of the semiconductor device substrate, is made of a resin material having at least one of a higher strength and a higher elongation than the resin material of the inner resin layers in the semiconductor device substrate.

3. (PREVIOUSLY PRESENTED) The semiconductor device substrate as set forth in claim 1, wherein resin material forming the outermost layer has a fracture strength of at least

90 MPa and an elongation of at least 10%.

4. (PREVIOUSLY PRESENTED) The semiconductor device substrate as set forth in claim 2, wherein resin material forming the outermost layer has a fracture strength of at least 90 MPa and an elongation of at least 10%.

5. (CURRENTLY AMENDED) A semiconductor device substrate, comprising:

a core substrate having, on both main surfaces of which, respective interconnect patterns extending through resin layers,

the core substrate being of a material having a heat expansion coefficient of 4.0 to 10.6 ppm/°C, the heat expansion coefficient closer to that of a semiconductor chip than respective heat expansion coefficients of resin layers and interconnect patterns inside the semiconductor device substrate; ~~and~~

a resin layer, of a material having at least one of a higher strength and a higher elongation than a resin material used for the resin layers inside the semiconductor device substrate, forming an outermost layer on each of the opposite main surfaces of the semiconductor device substrate, and

an outermost interconnect pattern of the semiconductor device substrate is coated by a resin layer forming an outermost layer of the semiconductor device substrate, and the outermost interconnect pattern having a land exposed through the outermost layer formed of the resin layer.

6. (PREVIOUSLY PRESENTED) The semiconductor device substrate as set forth in claim 5, wherein a further resin layer, under the resin layer forming the outermost layer of the semiconductor device substrate, is made of a resin material having at least one of a higher strength and a higher elongation than the resin material of the inner resin layers in the semiconductor device substrate.

7. (PREVIOUSLY PRESENTED) The semiconductor device substrate as set forth in claim 5, wherein resin material forming the outermost layer has a fracture strength of at least 90 MPa and an elongation of at least 10%.

8. (PREVIOUSLY PRESENTED) The semiconductor device substrate as set forth in claim 6, wherein resin material forming the outermost layer has a fracture strength of at least

90 MPa and an elongation of at least 10%.

9. (CURRENTLY AMENDED) A substrate for a chip, comprising:

a first resin layer forming an outermost layer on each of opposite main surfaces of the substrate coating an outermost interconnect pattern of the substrate, the outermost interconnect pattern having a land exposed through the outermost layer formed of the first resin layer;

a second resin layer underlying the first resin layer;

a third resin layer underlying the second resin layer; and

a core being of a material having a heat expansion coefficient of 4.0 to 10.6 ppm/°C, and underlying the third resin layer having, on both main surfaces, respective interconnect patterns between the core and at least one of the first resin layer, the second resin layer, and the third resin layer,

wherein at least one of the first resin layer and the second resin layer being of a material having at least one of a higher strength and a higher elongation than a material used for the third resin layer.

10. (PREVIOUSLY PRESENTED) The substrate according to claim 9, wherein material forming the first resin layer has a fracture strength of at least 90 MPa and an elongation of at least 10%.

11. (CURRENTLY AMENDED) A semiconductor device substrate comprised of a core substrate having, on both main surfaces of which, respective interconnect patterns extending through resin layers, wherein:

the core substrate being of a metal alloy having a heat expansion coefficient of 4.0 to 10.6 ppm/°C, the heat expansion coefficient closer to that of a semiconductor chip than the respective heat expansion coefficients of the resin layers and the interconnect patterns, and

a resin layer, forming an outermost layer of the semiconductor device substrate on each of the main surfaces thereof, of a material having at least one of a higher strength and a higher elongation than a resin material used for inner resin layers of the semiconductor device substrate and preventing cracking and deformation, of the semiconductor device substrate due to thermal stress occurring between two or more of the core substrate, the inner resin layers, and the interconnect patterns in the semiconductor device substrate,

an outermost interconnect pattern of the semiconductor device substrate is coated by

a resin layer forming an outermost layer of the semiconductor device substrate, and the outermost interconnect pattern has a land exposed through the outermost layer formed of the resin layer.

12. (PREVIOUSLY PRESENTED) The semiconductor device substrate according to claim 11, wherein the metal alloy being an iron-nickel alloy.

13. (CURRENTLY AMENDED) A substrate for a chip, comprising:

a first resin layer forming an outermost layer on each of opposite main surfaces of the substrate coating an outermost interconnect pattern of the substrate, the outermost interconnect pattern having a land exposed through the outermost layer formed of the first resin layer;

a second resin layer underlying the first resin layer;

a third resin layer underlying the second resin layer; and

a metal alloy core having a heat expansion coefficient of 4.0 to 10.6 ppm/°C and underlying the third resin layer having, on both main surfaces, respective interconnect patterns between the core and at least one of the first resin layer, the second resin layer, and the third resin layer,

wherein at least one of the first resin layer and the second resin layer being of a material having at least one of a higher strength and a higher elongation than a material used for the third resin layer.

14. (CURRENTLY AMENDED) A topology for a chip, comprising:

a first insulating layer forming an outermost layer on each of opposite main surfaces of a substrate coating an outermost interconnect pattern of the substrate, the outermost interconnect pattern having a land exposed through the outermost layer formed of the first resin layer;

a second insulating layer underlying the first insulating layer;

a third insulating layer underlying the second insulating layer; and

a metal alloy core having a heat expansion coefficient of 4.0 to 10.6 ppm/°C, and underlying the third insulating layer having, on both main surfaces, respective interconnect patterns between the metal alloy core and at least one of the first insulating layer, the second insulating layer, and the third insulating layer,

wherein at least one of the first insulating layer and the second insulating layer being of a

material having at least one of a higher strength and a higher elongation than a material used for the third insulating layer.

15. (PREVIOUSLY PRESENTED) The topology for a chip according to claim 14, wherein the metal alloy core being an iron-nickel alloy.

16. (NEW) A semiconductor device substrate, comprising:

a core substrate having a heat expansion coefficient of 4.0 to 10.6 ppm/°C; and

an outermost interconnect pattern of the semiconductor device substrate coated by a resin layer forming an outermost layer of the semiconductor device substrate, and the outermost interconnect pattern having a land exposed through the outermost layer formed of the resin layer.